REMARKS

By this Amendment, claims 2-5 are amended. Claims 1 and 6-15 remain in the application, although claims 5-15 were withdrawn from consideration by the Examiner based on the election of claims 1-4. Thus, claims 1-4 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

The specification and abstract have been carefully reviewed and revised in order to correct grammatical and idiomatic errors in order to aid the Examiner in further consideration of the application. The amendments to the specification and abstract are incorporated in the attached substitute specification and abstract. No new matter has been added.

Also attached hereto is a marked-up version of the substitute specification and abstract illustrating the changes made to the original specification and abstract.

In item 3 on page 2 of the Office Action, claims 1 and 2 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tomishima et al. (U.S. Patent Application Publication No. 2003/0007296). This rejection is respectfully traversed for the following reasons.

The present invention, as recited in claim 1, provides a standard voltage generation circuit comprising a standard voltage generation circuit body for generating a standard voltage (i.e., reference voltage), a standard voltage stabilization capacitor for stabilizing the standard voltage, and a standard voltage rapid stabilizer for rapidly stabilizing the standard voltage. Accordingly, the standard voltage rapid stabilizer of the present invention rapidly stabilizes a standard voltage that is generated by a standard voltage generation circuit body.

In contrast to the present invention, Tomishima et al. merely discloses a voltage down converter (VDC) circuit 600 for stabilizing an internal voltage Vdd. In item 3 on page 2 of the Office Action, the Examiner has interpreted the transistor QD1 (left hand side of Figure 16, hereinafter "left QD1") of Tomishima et al. as corresponding to the standard voltage generation circuit body of claim 1, and the transistor QD1 (right hand side of Figure 16, hereinafter "right QD1") of Tomishima et al. as corresponding to the standard voltage rapid stabilizer of claim 1. The Applicants respectfully submit that the

left QD1 and the right QD1 of Tomishima et al. do not constitute the invention of claim 1 of claim 1 for the following reasons.

The VDC 600 of Figure 16 consists of two VDCs, VDC601 and VDC602. The left QD1 is an element of the first VDC VDC601, and the right QD1 is an element of the second VDC VDC602. VDC601 and VDC602 are identical in structure, and the left QD1 of VDC601 is a current supply transistor QD1 for VDC601, while the right QD1 is a current supply transistor QD1 of VDC602 (see paragraph [0028] and Figures 3 and 16).

The left and right QD1s of Tomishima et al. merely supply a current Isup in the VCD 600 of Tomishima et al. A transistor QP32 (see top of Figure 16) acts as a switch in the VCD 600, and based on the switching operation of the transistor QP32, VDC601 and VDC602 can be forced to supply or not supply the supply current Isup when a variation in the internal voltage int. Vdd is noticed.

Accordingly, Toshima et al. merely stabilizes an internal voltage of the VCD 600 based on the mirror-structure of the left QD1 and the right QD1 and the current supply Isup which is forced out of at least one of the left QD1 and the right QD1.

However, neither the left QD1 nor the right QD1 generate a standard voltage for the VCD 600, or stabilize the standard voltage for the VCD 600.

Accordingly, the VCD of Toshima et al. clearly does not disclose or suggest a standard voltage generation circuit comprising a standard voltage generation circuit body for generating a standard voltage, a standard voltage stabilization capacitor for stabilizing the standard voltage, and a standard voltage rapid stabilizer for rapidly stabilizing the standard voltage, as recited in claim 1.

Therefore, claim 1 is clearly not anticipated by Toshima et al. since Toshima et al. fails to disclose each and every limitation of claim 1.

In item 5 on page 3 of the Office Action, claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ooishi (U.S. 6,191,994) in view of Tomishima et al.

Ooishi discloses a semiconductor device which includes two current supply circuits for supplying current to two internal circuits 2A and 2B via nodes N5 and N6, respectively. The two current supply circuits are identical in structure. The current supply circuit for supplying current to the internal circuit 2B includes a plurality of

PMOS transistors 17a-17x connected between the node N1, to which an external supply voltage is applied, and a node N6 for supplying the internal supply voltage to the internal circuit 2B. The current circuit for supplying current to the internal circuit 2B also includes a PMOS transistor 18 having a gate and a drain both connected to the gates of the transistors 17a-17x to generate a voltage to be applied to the gates of transistors 17a-17x, and a source connected to the node N1 (see Column 5, lines 55-63 and Figure 1).

The Examiner referred to the current mirror structure 17, 18 as rapidly stabilizing a standard voltage of the circuit of Ooishi. However, Ooishi merely discloses that consumption currents in transistors other than in the internal circuit are reduced (see Column 6, lines 40-60). That is, Ooishi does not disclose or suggest the current mirror structure 13, 14 or the current mirror structure 17, 18 as rapidly stabilizing the standard voltage of the circuit of Ooishi since Ooishi merely discloses reducing the amount of current that flows through transistors 13, 14 or 17, 18 to reduce the amount of current supplied to internal circuits 2A and 2B.

Accordingly, similar to Tomishima et al., Ooishi also clearly does not disclose or suggest a standard voltage generation circuit comprising a standard voltage generation circuit body for generating a standard voltage, a standard voltage stabilization capacitor for stabilizing the standard voltage, and a standard voltage rapid stabilizer for rapidly stabilizing the standard voltage, as recited in claim 1.

Therefore, no obvious combination of Tomishima et al. and Ooishi would result in the invention of claim 1 since Tomishima et al. and Ooishi, either individually or in combination, clearly do not disclose or suggest each and every limitation of claim.

Furthermore, it is submitted that the clear distinctions discussed above are such that a person having ordinary skill in the art at the time the invention was made would not have been motivated to modify Tomishima et al. and Ooishi in such as manner as to result in, or otherwise render obvious, the present invention as recited in claim 1. Therefore, it is submitted that the claim 1, as well as claims 2-7 which depend therefrom, are clearly allowable over the prior art as applied by the Examiner.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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